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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,119	11/28/2001	Sean B. Simmons	555255012299	1511

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,119	SIMMONS ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12,14-17,21-24 and 29* is/are rejected.

7)☒ Claim(s) *22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2-12, 14-17, 21-24 and 29 are pending in the instant application.

Response to Amendment

2. In view of the amendments to the claims filed September 15, 2005, the claim objections set forth in the first office action dated June 14, 2005 have been withdrawn.

3. New prior art rejections are set forth below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Critchlow (US 5276706 – previously cited).

Regarding claim 2, Critchlow discloses by figure 1 a synchronization (sync) signal detector comprising: a) a sync signal generator (36) for generating a reference sync signal (38); c) a waveform correlator (30) connected to the sync signal generator, the waveform correlator receiving a input signal (32 & 34); d) a peak detector (44) connected to the waveform correlator and the sampler; and e) a synchronization information calculator (46) connected to the waveform correlator and the peak detector, the synchronization information calculator providing data to one or more components (i.e. 49) external to the synchronization signal detector. The parabolic interpolator (fig. 1, ref. 46) is a synchronization information calculator because it calculates

synchronization information (48) which is provided to the voltage controlled oscillator for synchronization of the circuitry. Additionally, the VCXO (fig. 1, ref. 49) is not considered to be part of the main sync circuit, and therefore is considered to be external to the sync signal detector. Critchlow does not explicitly disclose b) a sampler connected between the sync signal generator and the waveform correlator. However, it is apparent from the disclosure that the output (38) of the sync signal generator is a digital signal because it is phase shifted by a symbol or sample portion according to the pattern rotator (37) (col. 7, lines 5-65). One skilled in the art is aware that the synchronization signal generator must contain some form of sampler to output digital data from the synchronization waveform. Therefore it would have been obvious to one having ordinary skill in the art at the time which the invention was made that a sampler is effectively present between the sync signal generator and the waveform correlator because both the pattern rotator and waveform correlator act upon digital signals which must be generated by a sampler.

Regarding claim 9, Critchlow discloses the limitations of claim 2 as applied above. Further, Critchlow discloses that the sync signal detector is implemented in a cellular telephone or communications system (abstract).

6. Claims 3-7 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Critchlow in view of Mimura et al (US 5617451; hereafter "Mimura").

Regarding claim 3, Critchlow discloses a synchronization signal detector comprising a) a sync signal generator, b) a sampler, c) a waveform correlator, and d) a peak detector as applied to claim 2 above. Critchlow discloses a demodulator or down converter (fig. 1, ref. 16) connected to the waveform correlator (fig. 1, ref. 30) and

configured to provide a demodulated output signal as an input to the waveform correlator, but does not explicitly disclose that a phase calculator and a frequency modulation demodulator providing an input signal to the waveform correlator. However, Mimura teaches by figure 1 a frequency modulation (col. 1, lines 10-11) receiver wherein the down converter comprises a phase calculator (31 & 32) to receive a frequency modulated input signal from the antenna (30A) and a frequency modulation demodulator (3) connected to the phase calculator. One skilled in the art is aware that to down convert and demodulate a received frequency modulation signal, a phase calculator or mixer must be applied to the received signal to remove the carrier frequency and the signal must be demodulated to recover the information. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the phase calculators and frequency modulation demodulator of Mimura in place of the generic down converter of Critchlow because it would allow the received signal carrier to be removed and signal information to be determined.

Regarding claim 4, Critchlow in view of Mimura disclose the limitations of claim 3 as applied above. Further, Critchlow discloses the sync signal detector implemented in a communication signal receiver (fig. 1).

Regarding claim 5, Critchlow in view of Mimura disclose the limitations of claim 4 as applied above. Further, Critchlow discloses a synchronization information calculator connected to the waveform correlator and the peak detector as applied to claim 1 above.

Regarding claim 6, Critchlow in view of Mimura disclose the limitations of claim 5 as applied above. Further, Critchlow discloses, as broadly as claimed, that the synchronization information (col. 8, lines 40-45) comprises a modulation index because it indexes the correct frequency to be utilized during demodulation of the modulated received signal.

Regarding claim 7, Critchlow in view of Mimura disclose the limitations of claim 5 as applied above. Further, Critchlow discloses that the synchronization information comprises a frequency offset (col. 8, lines 40-45).

Regarding claim 17, Critchlow in view of Mimura disclose the limitations of the claim as applied to claim 3 above.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Critchlow in view of Thomas et al (US 5754603; hereafter "Thomas").

Regarding claim 8, Critchlow discloses the limitations of claim 2 as applied above. Critchlow does not explicitly disclose that the waveform correlator and peak detector are implemented in a digital signal processor (DSP). However, Thomas teaches that a digital signal processor (DSP) can be utilized to easily implement correlation steps (col. 2, lines 35-40). In the method of Thomas, correlation is performed by a DSP (fig. 1, ref. 28). One skilled in the art is aware that a DSP can be utilized to execute computer readable program code to implement the steps of a correlation easily as taught by Thomas. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a DSP as

taught by Thomas for carrying out correlation and peak detection in the device of Puckette because the DSP provides an easy implementation of the device.

8. Claims 10-12, 14-16, 21, 24, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puckette (US 3654390 – previously cited) in view of Mimura.

Regarding claim 10, Puckette discloses a process for detecting a synchronization (sync) signal within an input signal (abstract), said process comprising the steps of: a) generating a version of the sync signal (fig. 1, ref. 12); b) correlating (fig. 2, refs. 21, 22, 24, and 25) the sync signal (fig. 2, ref. 15) with the input signal (fig. 2, ref. 10) to generate a correlation signal (fig. 2, output of 26); c) detecting or generating a correlation peak from the correlation signal (fig. 2, ref. 26); d) estimating a timing offset by the threshold detector (fig. 2, ref. 27; col. 3, lines 12-17) based on the correlation peak for use by step a); e) repeating step a) to generate a shifted version of the sync signal (fig. 1, ref. 13) using the timing offset (figs. 1 & 2, ref. 28) estimated in step d); and f) further processing the input signal based on the shifted version of the sync signal until the end of the input signal (col. 3, lines 17-25). Puckette does not explicitly disclose that the input signal (fig. 1, ref. 10) is a frequency modulated input signal which is phase calculated and frequency demodulated. However, one skilled in the art is familiar with frequency demodulating a frequency modulated input signal as taught by Mimura and applied to claim 3 above. One skilled in the art is aware that to down convert and demodulate a received frequency modulation signal, a phase calculator or mixer must be applied to the received signal to remove the carrier frequency and the signal must be demodulated to recover the information. Therefore, it would have been

obvious to one having ordinary skill in the art at the time which the invention was made to utilize the phase calculators and frequency modulation demodulator of Mimura in place of the generic down converter of Critchlow because it would allow the received signal carrier to be removed and signal information to be determined.

Regarding claim 11, Puckette in view of Mimura disclose the limitations of claim 10 as applied above. Further, Puckette discloses between steps e) and f), determining and outputting synchronization information (figs. 1 and 2, ref. 28; col. 2, lines 41-44).

Regarding claim 12, Puckette in view of Mimura disclose the limitations of claim 10 as applied above. Further, Puckette discloses that step a) consists of i) generating the sync signal utilizing a known timing offset because the timing offset is determined according to the phasing circuit (fig. 1, ref. 13) as disclosed (col. 2, line 40).

Regarding claim 14, Puckette in view of Mimura disclose the limitations of claim 10 as applied above. Further, Puckette discloses between steps e) and f), determining and outputting synchronization information (fig. 1, ref. 14; col. 2, lines 41-44).

Regarding claim 15, Puckette in view of Mimura disclose the limitations of claim 14 as applied above. Further, Puckette discloses that said synchronization information (figs. 1 and 2, ref. 28) comprises a frequency offset because it comprises the amount of disagreement or offset between the received sync signal and the generated sync signal (col. 3, lines 10-15 and lines 70-75).

Regarding claim 16, Puckette in view of Mimura disclose the limitations of claim 14 as applied above. Further, Puckette discloses that the synchronization information

(figs. 1 and 2, ref. 28) comprises a modulation index because it indexes the correct frequency to be utilized during demodulation of the modulated received signal.

Regarding claim 21, Puckette in view of Mimura disclose the limitations of the claim as applied to claims 10 and 16 above.

Regarding claim 24, Puckette in view of Mimura disclose the limitations of claim 21 as applied above. Further, Puckette discloses that step b) comprises shifting sampling points (fig. 1, ref. 13) within said known sync pattern (fig. 1, ref. 12) by the timing offset (fig. 2, ref. 28) determined from the waveform correlation (output of correlator; fig. 2, refs. 21, 22, 24 and 25) to create the shifted sync pattern (figs. 1 and 2, ref. 15).

Regarding claim 29, Puckette in view of Mimura disclose the limitations of claim 21 as applied above. Further, Puckette discloses that the synchronization information comprises a frequency offset because it comprises the amount of disagreement or offset between the received sync signal and the generated sync signal (col. 3, lines 10-15 and lines 70-75).

Allowable Subject Matter

9. Claims 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
November 14, 2005

jmp

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER